REMARKS

Claims 1-26 are pending and at issue. The office action rejects each of the pending claims based on a single patent to Tam, USPN 6,762,629. The applicants appreciate the examiner's review of the pending claims and consideration of the August 25, 2005 response, including the removal of the previous prior art rejections. The applicants address the rejections based on Tam below. First, however, the applicants traverse the finality of the office action.

PETITION TO REMOVE FINALITY

The examiner has made the office action final, because per the examiner the applicant's amendments necessitated the new grounds for rejection. This, however, is not the case. Only three claims were amended in the most-recent August 25 response, and each of those amendments merely added the already implied word "and" between the last and next to last claim recitations. As such, these amendments could not possibly have necessitated the new grounds for rejection. The finality of the office action is improper as a result. The applicants respectfully request removal of the finality.

ART REJECTIONS

Turning to the sole basis for the prior art rejection, Tam describes a method and apparatus for dynamically varying a clock frequency in a processor to adapt to VCC voltage changes. Tam describes sampling supply voltages at a plurality of locations and then communicating those supply voltages to a clock generator that adjusts the frequency of the generator's clock signals based on those supply voltages. Thus, Tam describes a system where the clock frequency is adjusted in response to a measured voltage. Power levels for the system are adjustable, but that adjustment is a result of the system changing the clock frequency in response to sample voltage values. As described:

> Embodiments of the present invention adapt the clock signal to voltage droops and fluctuations by dynamically adjusting the clock frequency based

> on sensed on-die voltage changes. For instance, when a droop is detected, the clock is slowed down to accommodate the reduced voltage level. Similarly, when the voltage recovery is detected, the clock frequency can be increased to enhance performance. Thus a mechanism in accordance with the present invention provides an ability to tailor a clock frequency based on realistic supply voltage levels and to alter the overall performance intelligently. Col. 3, ll. 44-54.

In contrast, claim 1 of the present application provides an article having instructions for measuring power usage on a machine, and sampling state data of that machine in response to a measured quantum of power usage. With the present application, for example, a system capable of measuring power may determine when a certain amount of power has been delivered to or consumed by the system. With such information, the system may determine whether or not a system state has changed since the last quantum of power was measured. If, for example, a program counter state is measured, and it is determined after multiple quantums of power have been used that the value of the program counter has not changed, then the system may determine that the code associated with that program counter may be hung up. Or, the system may determine that the code is particularly processor-intensive code that consumes a lot of power to execute. By not only measuring power, but also determining when a quantum of power has been used and then sampling state data in response to that measured quantum of power, the system may develop a power profile indicative of how much power is used by the system, a particular subsystem, or code executing on the system. The above examples are provided for illustrative purposes, not by way of limitation. However, they illustrate the different nature of the disclosures of Tam and that of the present application.

The office action points to columns 1 and 10 of Tam as teaching the subject matter of claim 1. Certainly figure 2 of Tam shows a plurality of voltage sensors. And as the above descriptions provide, frequency and thus power may be adjusted based on the values from these voltage sensors. Tam, for example, describes changing clock frequency in response to a

voltage droop or a voltage recovery. Focusing on the claimed subject matter, however, the office action points to nothing in Tam that teaches measuring power usage, determining when a quantum of power has been used, or sampling state data after it has been determined that the certain quantum of power has been used. To the contrary, Tam would appear to be directed to measuring voltage as an indicator of how the power should be adjusted. And even if Tam were to measure voltage and power, there is still no suggestion of sampling state data in response to the measurement of a quantum of power usage.

As Tam does not teach the subject matter of claim 1, the rejections of claim 1 and the claims depending therefrom are traversed.

In addition to the reasons outlined above, the applicants also address some of the claims depending from claim 1. With respect to dependent claim 8, which recites that the state date is a program counter, the office action points to frequency counters 612, 622, 632, and 642 as teaching the recited subject matter. The applicants respectfully disagree.

Tam describes these frequency counters as each receiving signals from these sensors. As described at column 10, ll. 59 et seq., these frequency counters count the number of oscillations or transitions in the signals from the sensors. There is no indication that these frequency counters are program counters. There is no indication that these frequency counters reflect where the system is in its instruction sequence. There is indeed no indication that these frequency counters reflect the execution of program code in any way. Therefore, the rejection claim 8 is separately traversed on these grounds as well.

With respect to dependent claim 24, which recites having further instructions that when executed on the machine, cause the machine to profile power usage of code executing on the machine, the office action points to the background portions of Tam and Figure 7B, which shows a method for adjusting clock frequency. The office action, in fact, points to nothing in Tam

as teaching or suggesting the profiling of the power usage of code that is executing on the machine.

What the office action highlights are descriptions of techniques for changing clock frequency, and thus power; there is no description of profiling the power used by particular code executing on a system. Referring the examiner to paragraph [0028] of the application, for some examples, the office action points to nothing in Tam as determining how much power particular code is using, determining how much power is being used by instructions and modules within that code, or profiling code with reference to historical sampled state data. Tam may describe measuring VCC voltage levels and adjusting frequencies in response, but the office action points to nothing that would allow the system to profile the power used by code executing on the machine. The rejection of claim 24 is separately traversed on these grounds.

For similar reasons to those outlined above with respect to claims 8 and 24, the rejection of dependent claim 25 is separately traversed as well.

With respect to the rejection of dependent claims 26, which recites that the state data comprises a stack pointer, current memory usage, a number of instructions executed, or a number of accesses to a memory storage, the office action concludes that Tam discloses a number of accesses to a memory storage. The office action, however, points to nothing in Tam as describing accessing memory storage in response to the measurement of a quantum of power usage. At best, it would appear that Tam accesses the clock in response to a measured voltage value. The rejection of claim 26 is thus separately traversed.

Claim 10 is a method claim similar to claim 1 and that recites:

> A method of profiling code executable on a machine, comprising:
> measuring power usage on the machine; and

> in response to a measured quantum of power usage, sampling state data on the machine.

For at least the reasons outlined above, the rejection of claim 10 is traversed.

Further still, the applicants address the recitations of various claims depending from claim 10. Claim 11 recites measuring power delivered to at least one of the plurality of subsystems. Claim 12 recites measuring power consumed by at least one of the plurality of subsystems. As the application recognizes, there can be a difference between the power delivered to a subsystem and the power consumed by that subsystem. The office action points to figure 1 and units 105, 112, and 116 of the Tam as teaching the recitations of these claims. The applicants respectfully respond that there is nothing in these figures or the descriptions thereof that teaches techniques for differentiating between power delivered to a system and power consumed by that system, as set forth in the claims. The office action's rejections of these dependent claims are improper and thus traversed.

As amended, claim 20 recites:

> An apparatus comprising:
>
> a power measurement module capable of measuring power usage in the apparatus and capable of determining when a quantum of power has been used; and
>
> a power sampling module coupled to the power measurement module for sampling state data of the apparatus in response to a determination that the quantum of power has been used.

As noted above, the office action nowhere describes where Tam teaches determining when a quantum of power has been used. Furthermore, as noted above, Tam does not teach sampling state data in response to a determination that the quantum of power has been used. Thus for at least the reasons outlined above, the rejection of claim 20 has been traversed. Claim 20 and the claims depending therefrom are in condition for allowance.

In light of the foregoing, the applicants respectfully submit that each of the pending claims is in condition for immediate allowance. Expedited confirmation of the same is respectfully requested.

It is believed that no fee is due. However, the Commissioner is authorized to charge any fee deficiency required by this paper to Deposit Account No. 13-2855.

Dated: November 21, 2005

Respectfully submitted,

By _____

Paul B. Stephens
Registration No.: 47,970
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant